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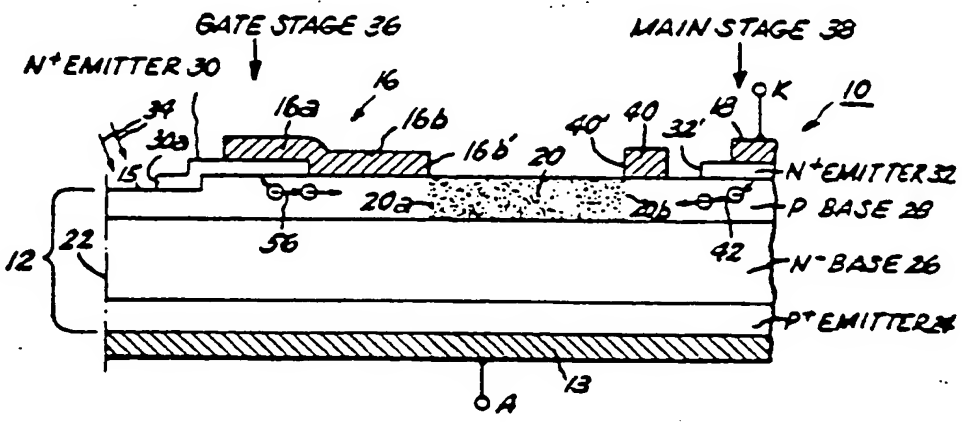

(57) Abstract

A multistage amplifying thyristor (10) incorporates integral current control resistor regions (20, 20') between adjacent thyristor stages (36, 36', 102) for limiting turn-on current in all but the main thyristor stage (38'). The thyristor (10) is essentially immune from di/dt turn-on failure without the need for external circuitry to limit di/dt in the thyristor (10). Modulation of the current control resistor region (20, 20') during turn-on is prevented by adequately spacing (110, 112, 120, 122) or shielding (38, 40) the region from the emitter (30, 32) of each thyristor stage (36, 36', 102) as well as by adequate spacing (106, 116) or shielding (72') of the resistor region (20, 20') from a portion of the lowermost emitter region (30, 32) containing a turn-on plasma (60) of the preceding thyristor stage (36, 36', 102).

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CONTROLLED TURN-ON THYRISTOR

Background of the Invention

The present invention relates to multistage amplifying thyristors with at and main stages and, more particularly, relates to a multistage amplifying thyristor in which the peak turn-on current in the gate and any intermediate thyristor stages is limited during thyristor turn-on.

Conventional multistage amplifying thyristors include gate and main stages and may include one or more intermediate stages. The reason for including several stages in a thyristor is to permit turn-on of the thyristor with a gate signal of very low energy. For example, a light triggered thyristor (LTT) must rely upon a minute amount of light energy (typically on the order of about 20 nanojoules) to turn on the thyristor. This is possible since the light energy turns on only a gate thyristor stage which is highly-sensitive but of low current rating and which, in turn, turns on any intermediate thyristor stage. Successive turn-on of the various thyristor stages continues until turn-on of the main thyristor stage is turned on.

A significant limitation of conventional multistage amplifying thyristors is that the rate of turn-on, or di/dt, of such thyristors used in typical circuits must be controlled by external circuit devices in order to prevent thermal stresses in the thyristor from destroying the thyristor. For instance, a typical high voltage direct current transmission system utilizing thyristors for alternating current-to-direct current conversion incorporates relatively expensive saturable reactors. This type of reactor presents a

temporary, high inductive impedance to turn-on current flow in a thyristor, but rapidly falls off in its level of inductive impedance upon steady state thyristor operation.

A published approach to designing a thyristor with enhanced immunity from di/dt thermal stress failure, known as the controlled turn-on approach, is to incorporate into a multistage amplifying thyristor current control resistor regions, one between each pair of adjacent thyristor stages. These current control resistor regions are intended to reduce turn-on, or di/dt, thermal stress in a thyristor by functioning to, first, reduce the current in each preceding or prior turned-on thyristor stage and, second, reduce the duty cycle of each preceding thyristor stage. The subject approach is described in detail, for example, in an article by VAK Temple (the present inventor) entitled "Controlled Turn-on Thyristors" published in IEEE Transactions on Electron Devices, Vol. ED-30 (July 1983) at pages 816-824, the entirety of this article being incorporated herein by reference.

The foregoing Temple article describes successful performance of 5 kilovolt thyristors that were tested to a 600 volt level. Subsequent testing of thyristors such as described in the Temple article by the present inventor has shown the occurrence of turn-on failure, due to thermal stresses, at about the 2000 volt level. Further investigation into the controlled turn-on approach described in the Temple article has revealed that certain considerations, not taken into account in the investigation described in the article, are a factor in causing turn-on failure at about the 2000 volt level. The present invention

addresses these considerations and results in a multi-stage amplifying thyristor successfully exhibiting controlled turn-on at considerably higher voltages than heretofore attainable.

In general terms, the considerations not addressed in the Temple article are centered around the decrease in resistance value of the current control resistor regions incorporated into a thyristor, due to what is known in the art as a "modulation" effect in such resistor regions. It is important to note that these resistor regions comprise semiconductor material of nominal doping concentration and of either P- or N-conductivity type. The increase in either majority or minority carrier concentration in the current control resistor regions results in modulation, or lowering, of the resistance of such regions. This is readily appreciated in the case of increased majority carrier concentration due to the overall increase in concentration of majority carriers; however, in the case of increased minority carrier concentration, an additional phenomenon known in the art as the principle of quasi-neutrality is involved. In accordance with this principle, the concentration of majority carriers in a semiconductor region increases to roughly that of the minority carrier concentration, preventing unduly high electric fields from occurring in the thyristor.

The Temple article points out that within a multistage amplifying thyristor, there are sources of mobile carriers (in particular, the cathode emitter layers of the various thyristor stages) that increase the current carrier level in the current control resistor regions, unless these regions are sufficiently spaced or otherwise shielded from such sources of

carriers. The present invention is directed to a thyristor design in which further sources of mobile carriers, not recognized at the time of publication of the Temple article, are spaced or shielded from such sources of mobile carriers by an extent sufficient to minimize modulation of the current control resistor regions.

Summary of the Invention

Accordingly, it is a principal object of the present invention to provide a multistage amplifying thyristor with a reliable turn-on characteristic.

It is a further object of the invention to provide a multistage amplifying thyristor that is essentially immune from di/dt failure.

It is yet another object of the invention to provide a multistage amplifying thyristor with improved current control resistor regions that may be fabricated using conventional processing techniques.

In carrying out the objects of the invention, a multistage amplifying thyristor is provided, which includes a semiconductor body, a first emitter electrode, inner and outer stage emitter electrodes, and a current control resistor region. The semiconductor body, in preferred form, comprises a P^+ emitter layer, an N^- base layer atop the P^+ emitter layer, a P base layer atop the N^- base layer, an inner stage N^+ emitter layer atop the P base layer, and an outer stage N^+ emitter layer atop the P base layer and which is adjacent to and situated in, what is referred to herein as, an "outward" direction from the inner stage N^+ emitter layer.

The first emitter electrode underlies the P^+ emitter layer. The inner stage emitter electrode in a first part overlies the inner stage N^+ emitter layer and in a second part, situated outwardly from the first part, overlies the P base layer. The outer stage emitter electrode overlies the outer stage emitter layer. The current control resistor region constitutes a portion of the P base layer having its inner side extending as far as an outward edge of the inner stage emitter electrode and having its outward side extending as far as a recombination ring.

The current control resistor region has an unmodulated resistance value selected to limit to a safe level the turn-on current in each preceding thyristor stage. To minimize modulation of the current control resistor region during turn-on of the thyristor, an outer edge of the inner stage emitter electrode extends outwardly by a predetermined distance of at least about the greater of one thickness of the semiconductor body and two ambipolar diffusion lengths in the N^- base layer from any of:

an inner edge of the first stage emitter layer,

an outer edge of a turn-on plasma beneath the inner stage N^+ emitter layer, and

an outer edge of the first stage N^+ emitter layer.

Utilizing the above-described spacing of the current control resistor region from the first stage N^+ emitter layer, hole carrier injection from a portion of P^+ emitter layer situated beneath the first stage emitter layer is prevented from modulating the current control resistor region.

Brief Description of the Drawings

The features of the invention deemed to be novel are defined in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof may be best understood with reference to the following description when read in conjunction with the accompanying drawings, in which:

Figure 1 is a cross-sectional view of a portion of a thyristor incorporating features of the present invention;

Figure 2 is a schematic electrical circuit equivalent of the thyristor of Figure 1;

Figure 3 depicts the thyristor of Figure 1 and illustrates a source of mobile carriers that may result in unwanted modulation;

Figures 4A-4C depict variations of the thyristor of Figure 1 and illustrate different arrangements for spacing a current control resistor region from a first stage N^+ emitter layer of the thyristor, which spacing minimizes modulation of the current control resistor region;

Figure 5 depicts a further thyristor of the present invention incorporating an intermediate stage and indicates exemplary dimensions of various parts of the thyristor; and

Figure 6 is a fragmentary view of a current control resistor region that may be used in the Figure 1 thyristor, illustrating, in particular, a multi-zoned current control resistor region for equalizing thermal stresses in the various zones of the region.

Detailed Description of the Preferred Embodiments

Depicted in Figure 1 is a multistage amplifying thyristor 10 incorporating features of the present invention. Thyristor 10 includes a semiconductor body 12, such as silicon, a first emitter electrode 13, inner and outer stage emitter electrodes 16 and 18, respectively, and a current control resistor region 20. As viewed from above in Figure 1, thyristor 10 is circular in shape, by way of example, with a center illustrated in Figure 1 as center line 22. Inner and outer stage emitter electrodes 16 and 18, respectively, appear, as viewed from above in Figure 1, as annular in shape.

Semiconductor body 12 includes a P^+ emitter layer 24, N^- base layer 26 atop emitter layer 24, P base layer 28 atop base layer 26, an N^+ emitter layer 30 atop base layer 28, and an N^+ emitter layer 32 atop base layer 28 and which is adjacent to and situated in an outward direction from emitter layer 30, an "outward" direction signifying herein radially outward from center line 22. Depression 15 in P base layer 28, into which an inner edge 30a of N^+ emitter layer 30 extends, constitutes a gate area onto which radiation, such as light radiation 38, impinges for initiating turn-on of thyristor 10. N^+ emitter layer 30 constitutes the emitter of an inner thyristor stage 36, comprising a gate thyristor stage, while emitter layer 32 constitutes the emitter of an outer thyristor stage 38, that may comprise an intermediate or a main thyristor stage.

First emitter electrode 13 underlies P^+ emitter layer 24 and is designated "A", for "anode". Inner stage emitter electrode 16 in a first part 16a

overlies emitter layer 30 and in a second part 16b, situated outwardly from first part 16a, overlies P base layer 28. Main stage emitter electrode 18 overlies N^+ emitter layer 32 and is designated "K" for "cathode" The foregoing electrodes 13, 16 and 18 preferably comprise aluminum.

Further included in thyristor 10 is a recombination ring 40, such as aluminum, the purposes of which are elaborated on below.

Current control resistor region 20 constitutes a portion of P base layer 28 having its inner side 20a extending as far as an outward edge 16b' of inner stage emitter electrode 16 and having its outward edge 20b extending as far as an inner edge 40' of recombination ring 40.

Current control resistor region 20 has an unmodulated resistance between inner and outer sides 20a and 20b that is selected to limit to a safe level the turn-on current in the preceding, or gate stage 36, of thyristor 10. Selection of an appropriate value for the unmodulated resistance of resistor region 20 is discussed in the above-referenced Temple article. Fabrication of resistor region 20 is suitably accomplished by providing a suitable spacing between inner and outer resistor sides 20a and 20b without there being a need to specially alter the doping level (and, hence, resistivity) of P base layer 28. Alternatively, the doping concentration of resistor region 20 can be specially adjusted by ion implantation of suitable dopant, for example, whereby the separation between resistor sides 20a and 20b can be controlled independently of the doping level of the remainder of P base layer 28.

The purposes of current control resistor region 20 can be better understood with reference to the Figure 2 illustration of electrical circuit 50, which is the circuit equivalent of thyristor 10 of Figure 1. Gate and main thyristors 52 and 54, respectively, of electrical circuit 50 correspond to the gate and main stages 36 and 38, respectively, of thyristor 10, while the interstage series resistance R_s between thyristors 52 and 54 corresponds to the net device resistance between inner and outer stage emitter electrodes 16 and 18, respectively, of thyristor 10.

Interstage resistance R_s in circuit 50 provides two protective features in circuit 50: first, it limits current flow in gate thyristor 52 while main thyristor 54 is turned on, and, second, it reduces the duration of time that gate thyristor 52 conducts current when thyristor 10 is turning on, since current through main thyristor 54, once this thyristor is turned on and thus in a low impedance state, is favored over current through gate thyristor 52, which must flow through interstage resistance R_s.

Interstage resistance R_s contains components that are modulated during turn-on of circuit 50 (corresponding to turn-on of thyristor 10) to reduce the resistance value of R_s during this period of time. It is preferred that the modulated component of R_s not exceed about 10 percent of the unmodulated R_s value, although modulation as high as about 20 percent is believed to be acceptable.

The modulated components of resistance R_s can be understood by considering the analogous structure of thyristor 10 corresponding to resistance R_s of circuit 50. The thyristor 10 equivalent of resistance R_s

constitutes the net resistance between inner and outer stage emitter electrodes 16 and 18 as measured with emitter electrodes 16 and 18 free-floating in potential. Such net resistance contains modulated components during turn-on of thyristor 10 which are due, for example, to injection into P base layer 28 from N^+ emitter layer 30 of electrons depicted by path 56 and injection into P base layer 28 of electrons depicted by path 42 from N^+ emitter layer 32. To prevent electrons in path 42 from reaching resistor region 20 and modulating such region, recombination ring 40 removes electrons 42 in path from P base layer 28 in its function as a carrier recombination region. Even with recombination ring 40 present, spacing of inner edge 40' of recombination ring 40 from inner edge 32' of N^+ emitter layer 32 by at least about two minority carrier diffusion lengths in P base layer 28 is desirable.

Recombination ring 40 is also desirable for homogenizing the current transferred from gate stage 36 to main stage 38 of thyristor 10 during device turn-on. Ring 40, however, may be deleted from thyristor 10 as long as adequate spacing is provided between N^+ emitter layer 32 and current control resistor region 20, spacing of about three minority carrier diffusion lengths in P base layer 28 being suitable, by way of example.

The above-referenced Temple article points out that modulation of a current control resistor region may occur as a result of carrier injection from gate and main stage emitter layers into a P base layer (see the Temple article at page 823, Fig. 12 (c) and discussion thereof). The Temple article indicates

successful attainment of the objective of safe turn-on of a thyristor, but this was verified only at the 600 volt level for a 5 kilovolt device (see the Temple article page 819, seventh paragraph). Further thyristor testing and development has shown that modulation in current control resistor region 20 from a source of carriers other than N^+ emitter layers 30 and 32 must be taken into account.

An additional source of carriers that may result in modulation of current control resistor region 20 is illustrated in Figure 3, depicting the same view of thyristor 10 as shown in Figure 1, and, further, schematically illustrating a turn-on plasma 60 beneath N^+ emitter layer 30. Plasma 60 comprises electrons in path 62 injected from N^+ emitter layer 30 into P^+ emitter layer 24 and the returning holes in path 64 injected from P^+ emitter layer 24. The concentration of holes and electrons in plasma 60 is typically about 10^{17} per cubic centimeter for each type of current carrier. Functionally, plasma 60 is the portion of gate stage 36 that turns on when turn-on radiation 34, such as light, impinges upon gate depression 15 so as to generate hole-electron pair turn-on current. Some portion of hole current 66 from turn-on plasma 60 does not remain confined to the high density plasma, but instead becomes attracted to the current control resistor region 20. This attraction occurs because main stage emitter electrode 18 is typically biased to several thousand volts prior to turn-on of main stage 38, while, once gate 36 has turned on, inner stage emitter electrode 16 falls off in voltage intensity due to its low impedance connection, via turn-on plasma 60, to emitter electrode 13.

To counteract the tendency of holes in path 66 from entering and thus modulating current control resistor region 20, adequate spacing between turn-on plasma 60 and the current control resistor region is provided as depicted in Figure 4A, illustrating the same view as Figure 1. In particular, modulation of region 20 by holes in path 66 is avoided if outer edge 16b' of first stage emitter electrode 16 is spaced from an outer edge 70 of turn-on plasma 60 by a predetermined distance 72 of at least about the greater of one thickness of semiconductor body 12 and two ambipolar diffusion lengths (a standard design parameter) in N^- base layer 26. More conservative values for predetermined distance 72 are at least the greater of any of: two thicknesses of semiconductor body 12 and two ambipolar diffusion lengths in N^- base layer 26; two body thicknesses and three ambipolar diffusion lengths in layer 26; three body thicknesses and two ambipolar diffusion lengths in layer 26; and three body thicknesses and three ambipolar diffusion lengths in layer 26. The location of outer edge 74 of turn-on plasma 60 may be readily determined according to known principles in the art. An alternative spacing arrangement, shown in Figure 4B, is to space inner stage emitter electrode outer edge 16b' from an outer edge 74 of N^+ emitter layer 30 by a predetermined distance 72', which is of equal measure to predetermined distance 72 (indicated in Figure 4A). A further alternative spacing arrangement, shown in Figure 4C, is to space first stage emitter electrode outer edge 16b' from inner edge 76 of N^+ emitter layer 30 by a predetermined distance of 72', which is of equal measure to predetermined distance 72 (indicated in

Figure 4A). In selecting one of the spacing arrangements of Figures 4A-4C, it is a general consideration that the longer part 16b (of inner stage emitter electrode 16) is, the less likely it is for resistor region 20 to be undesirably modulated.

By way of example and not limitation, a 4.5 kilovolt light triggered thyristor 100, shown in Figure 5, was constructed in accordance with the present invention. Thyristor 100 includes an intermediate stage 102, corresponding to main stage 38 of thyristor 10 (Fig. 1). Light triggered thyristor 100 exhibited safe turn-on at the 4 kilovolt level with a di/dt value of about 450 amps per microsecond and with heat sink temperatures on different testing runs from 38 to 90° Centigrade. The tested thyristor had the following dimensions: radial distance 104 of 25 mils (0.025 inch); radial distance 106 (which includes distance 104) of 65 mils; and radial distances 108, 110, 112, 114, 116, 118, 120 and 122 of, respectively, 120 mils, 130 mils, 140 mils, 165 mils, 190 mils, 275 mils and 288 mils. The approximate resistance of current control resistor region 20 and 20' was, respectively, 98 ohms and 50 ohms.

If the amperage rating of thyristor 10 (Fig. 1) is very high, it is desirable to construct current control resistor region 20 in such a way as to more evenly spread the thermal stresses radially across the region. A preferred technique for accomplishing this is illustrated in Figure 6, depicting a fragmentary view of a modified region 20". This region includes first and second zones 110 and 112, respectively, with zone 112 being located outwardly of zone 110 and being thinner, and thus of higher resistance, than zone 110.

Zone 112 may be implemented, for example, by an etch step (not illustrated) that removes an upper portion of P base layer 28 down to level 114. This etch step may advantageously be carried out simultaneously with the etch step for gate depression 15 of gate stage 36 of thyristor 10 (Fig. 1). Zones 110 and 112 dissipate approximately the same amount of heat per unit volume as each other since the higher $(\text{current})^2 \times \text{resistance}$ heating of zone 112 is dissipated in a larger volume, zone 112 being of larger volume since it is located radially outward of zone 110.

Although not illustrated, current control resistor zone 20 may also be implemented as a series of zones of increasing resistance with increasing radial spacing. This could be accomplished, for example, by providing a series of successively thinner zones in a current control resistor region extending in the outward direction. As an alternative to utilizing thinner zones for higher resistance, zones of higher resistance could be implemented by ion implantation of suitable dopant, with a high resistance zone having a low dopant concentration, for example.

Fabrication of the above-described thyristors may be carried out with conventional semiconductor device processing techniques and will be within the purview of those skilled in the thyristor art in light of the present specifications.

The foregoing describes a multistage amplifying thyristor incorporating built-in or integrated current control resistor regions between adjacent thyristor stages for limiting current in all but the main thyristor stage. The thyristor accordingly achieves essential immunity from di/dt turn-on failure

without the need for external circuitry to limit the di/dt value of the thyristor.

While only certain preferred features of the invention have been shown by way of illustration, many modifications and changes will occur to those skilled in the thyristor art. For example, complementary thyristors could be made in which P-conductivity type semiconductor material is substituted for N-conductivity type material, and vice-versa. It is, therefore, to be understood that the appended claims are intended to cover the foregoing and all such modifications and changes as fall within the true spirit and scope of the invention.

CLAIMS:

1. In a multistage amplifying thyristor including a semiconductor body, a first emitter electrode, inner and outer stage emitter electrodes, and a current control resistor region;

said semiconductor body comprising a first emitter layer, a first base layer atop said first emitter layer, a second base layer atop said first base layer, an inner stage emitter layer atop said second base layer, and an outer stage emitter layer atop said second base layer and which is adjacent to and situated in an outward direction from said inner stage emitter layer;

said first emitter electrode underlying said first emitter layer;

said inner stage emitter electrode in a first part overlying said inner stage emitter layer and in a second part, situated outwardly from said first part, overlying said second base layer;

said outer stage emitter electrode overlying said outer stage emitter layer;

said current control resistor region constituting a portion of said second base region defined on an inner side by an outward edge of said inner stage emitter electrode and extending towards but spaced from said outer stage emitter layer;

said current control resistor region having an unmodulated resistance selected to limit to a safe level the turn-on current in each preceding amplifying thyristor stage;

the improvement to said multistage amplifying thyristor, in combination with the foregoing, for

minimizing modulation of said current control resistor region during turn-on of the thyristor, comprising:

an outer edge of said inner stage emitter electrode extending outwardly by a predetermined distance of at least about the greater of one thickness of said semiconductor body and two ambipolar diffusion lengths in said first base layer from any of:

an inner edge of said first stage emitter layer,

an outer edge of turn-on plasma beneath said inner stage emitter layer, and

an outer edge of said first stage emitter layer.

2. The invention of claim 1 wherein said predetermined distance by which said outer edge of said inner stage emitter electrode extends outwardly comprises at least about the greater of two thicknesses of said semiconductor body and two ambipolar diffusion lengths of said first base region.

3. The invention of claim 1 wherein said predetermined distance by which said outer edge of said inner stage emitter electrode extends outwardly comprises at least about the greater of two thicknesses of said semiconductor body and three ambipolar diffusion lengths in said first base region.

4. The invention of claim 1 wherein said predetermined distance by which said outer edge of said inner stage emitter electrode extends outwardly comprises at least about the greater of three thicknesses of said semiconductor body and two ambipolar diffusion lengths in said first base region.

5. The invention of claim 1 wherein said predetermined distance by which said outer edge of said inner stage emitter electrode extends outwardly comprises at least about the greater of three thicknesses of said semiconductor body and three ambipolar diffusion lengths in said first base region.

6. The invention of claim 1 wherein said outer edge of inner stage emitter electrode extends outwardly by said predetermined distance from any of:

an outer edge of a turn-on plasma beneath said inner stage emitter layer, and

an outer edge of said first stage emitter layer.

7. The invention of claim 1 wherein said outer edge of said inner stage emitter electrode extends outwardly by said predetermined distance from an outer edge of said first stage emitter layer.

8. The invention of claim 1 wherein said control resistor emitter region comprises at least two zones with the outer zone having a higher resistance than the inner zone.

9. The invention of claim 8 wherein said outer zone of said current control resistor region is thinner than said inner zone of said current control resistor region.

FIG. 1

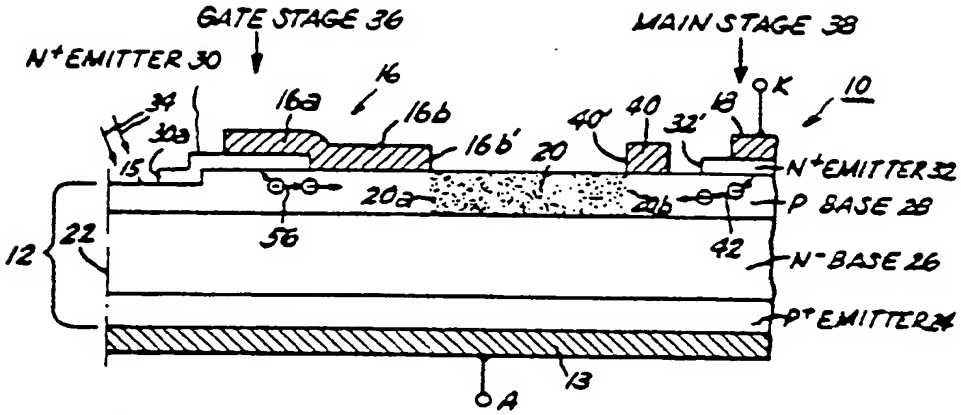


FIG. 2

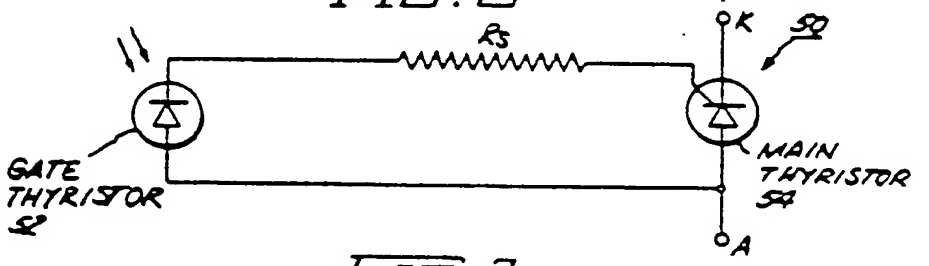


FIG. 3

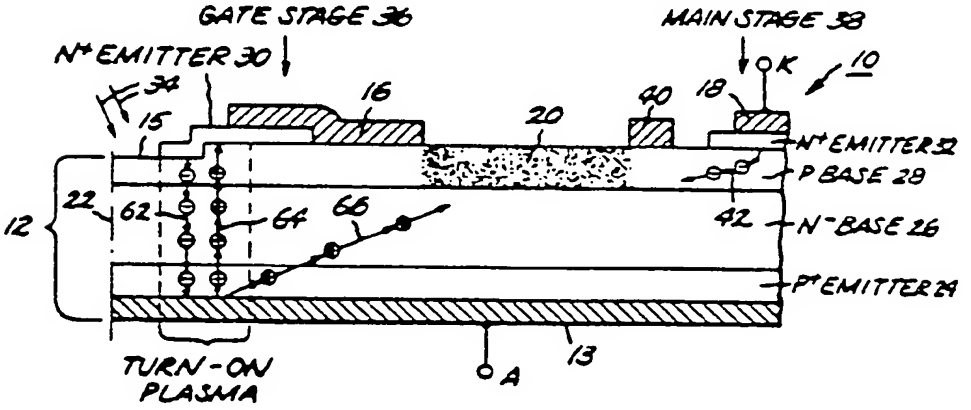


FIG. 4A

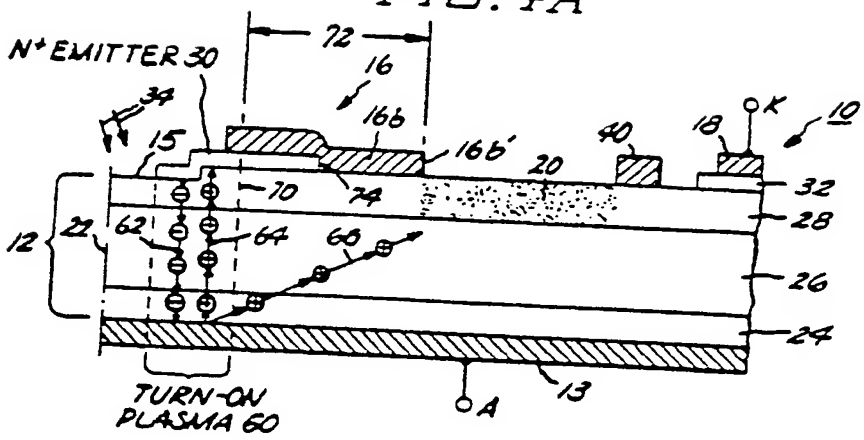


FIG. 4B

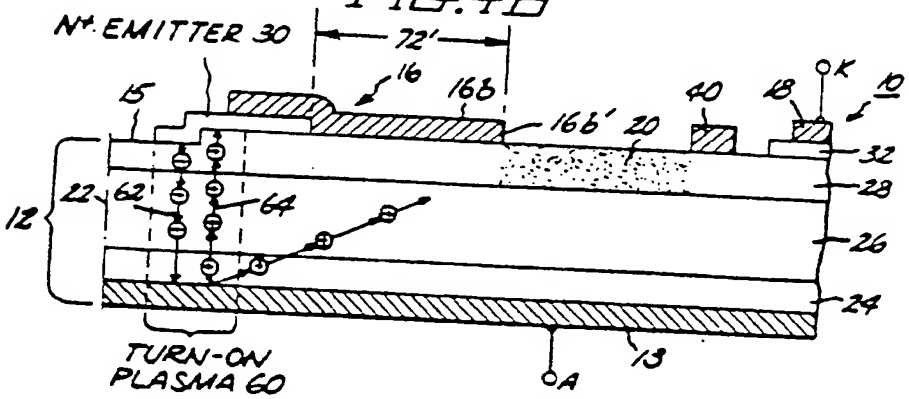
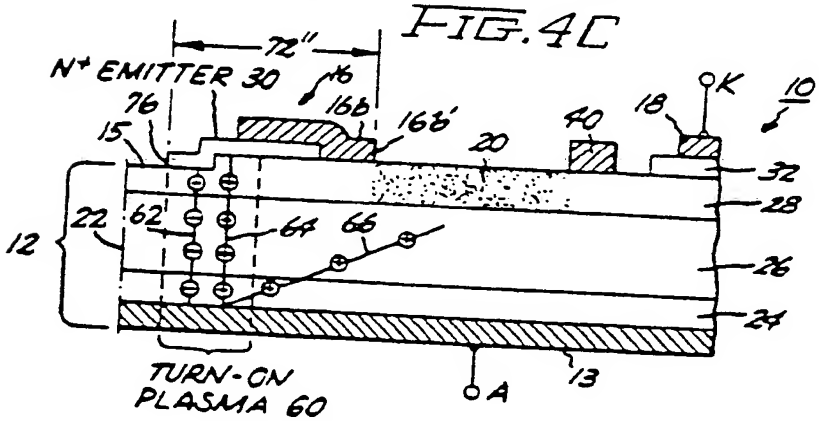


FIG. 4C



SUBSTITUTE SHEET

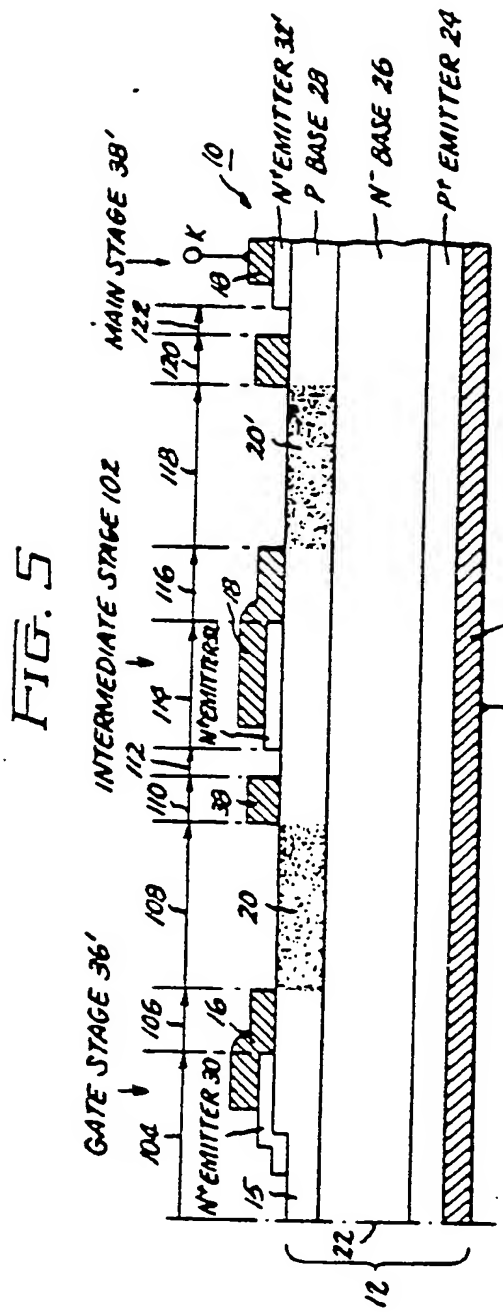


FIG. 5

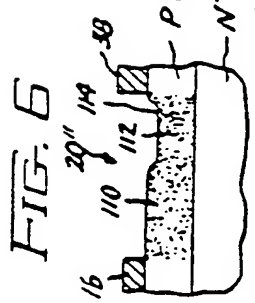


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US85/01002

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 3

According to International Patent Classification (IPC) or to both National Classification and IPC 4

357/20, 38, 51, 55, 64; H01L 29/74

II. FIELDS SEARCHED

Minimum Documentation Searched 4

Classification System	Classification Symbols
U.S.	357/20, 38, 51, 55, 64

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 5

III. DOCUMENTS CONSIDERED TO BE RELEVANT 14

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No. 18
Y	US, A, 3, 246, 172 PUBLISHED 12 APRIL 1966, SANFORD	1-9
Y	US, A, 3, 248, 677 PUBLISHED 26 APRIL 1966, HUNTER ET AL.	1-9
Y	US, A, 3, 408, 545 PUBLISHED 29 OCTOBER 1968, SEE FIGURES 8, 9, AND 10, DECECCO ET AL.	1-9
A	US, A, 3,671, 821, PUBLISHED 20 JUNE 1972, NAKATA ET AL.	1-9
Y	US, A, 3, 967, 294 PUBLISHED 29 JUNE 1976, TAKASE ET AL.	1-9
X	US, A, 4, 012, 761 PUBLISHED 15 MARCH 1977, FERRO ET AL.	1-9
Y	US, A, 4, 261, 001 PUBLISHED 07 APRIL 1981, TEMPLE	1-9

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search 2	Date of Mailing of this International Search Report 2
15, AUGUST 1985	21 AUG 1985
International Searching Authority 1	**Signature of Authorized Officer 20**
ISA/US	

Form PCT/ISA/210 (second sheet) (October 1981)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

X	US, A,4,281, 336 PUBLISHED 28 JULY 1981, SOMMER ET AL.	1-9
Y	US, A, 4, 500, 901 PUBLISHED 19 FEBUARY 1985, SOMMER ET AL.	1-9
Y	N, IEEE TRANSACTIONSON POWER APPARATUS AND SYSTEMS, VOLUME PAS-101, NUMBER 7, JULY 1982, PAGES 1-6, SEE PAGE 2, RIGHT COLUMN	1-9

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ... ... because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ...., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international sparch can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International search report covers all searchable claims of the International application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the International application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.